UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/621,110	07/21/2000	Charles Cohn	6-4	4412

7590 09/12/2002

Docket Administrator Romm 3C-512
Lucent Technologies Inc
600 Mountain Avenue
P O Box 636
Murray Hill, NJ 07974-0636

EXAMINER
LUU, CHUONG A

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 09/12/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/621,110	Applicant(s) COHN ET AL.	
	Examiner Chuong A Luu	Art Unit 2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *13-16* is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *8* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Prosecution Application

The request filed on July 31, 2002 for a Continued Prosecution Application (CPA) under 37 CFR 1.53(d) based on parent Application No. 09/621,110 is acceptable and a CPA has been established. An action on the CPA follows.

PRIOR ART REJECTIONS

Statutory Basis

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The Rejections

Claims 1, 6-8, 10 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Broadbent (U.S. 5,063,175) in view of Manteghi (U.S. 6,228,683 B1)

Broadbent discloses a method for manufacturing a planar electrical interconnection system suitable for an integrated circuit with

(1) (a) forming a substrate (30) having an insulating layer (first dielectric layer) (31), a conductive layer (36) having a first region insulated from a second region and located above the insulating layer (first dielectric layer) (31), and an insulating layer

(second dielectric layer) (37) above the conductive layer (36), the insulating layer (second dielectric layer) (37) having grooves (cavity) (41) wherein the first and second regions are exposed with the grooves (cavity) (41) and the first region insulated from the second region by a third dielectric layer;

(7) (a) forming an insulating layer (first dielectric layer) (31), on a substrate (30);

(b) forming a conductive layer (36) having a first region insulated from a second region above the insulating layer (first dielectric layer) (31);

(c) an insulating layer (second dielectric layer) (37) above the conductive layer (36);

(d) forming grooves (cavity) (41) in the insulating layer (second dielectric layer) (37) to expose the first and second regions of the conductive layer and (36) the first region insulated from the second region by a third dielectric layer (see Figures 3a-3j);

(8) wherein steps (a), (b), and (c) occur prior to step (d) (see Figures 3a-3j);

Broadbent teaches the above outlined features except for using lead to connect an integrated circuit to the first exposed region and interconnecting a second lead of the integrated circuit to the exposed second region. However, Manteghii discloses a high density leaded ball-grid array package with **(1).....**(b) interconnecting a first lead of an integrated circuit to the first exposed region and interconnecting a second lead of the integrated circuit to the exposed second region; **(6)** further comprising forming multiple interconnections between the integrated circuit chip and the conductive layer; **(7).....**(d) coupling a first lead of the integrated circuit chip to the the exposed first region and coupling a second lead of the integrated circuit to the exposed second

region, (see Figure 2A); **(10)** (e) forming plated through holes in the substrate (see column 1, lines 23-43); **(12)** further comprising coupling the integrated circuit chip to the substrate (see Figure 2A). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the above teachings to manufacture a semiconductor interconnection to improve its performance.

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Broadbent (U.S. 5,063,175) in view of Manteghi (U.S. 6,228,683 B1) and further in view of Plepys et al. (U.S. 6,140,707)

Broadbent and Manteghi teach the above outlined features except for bond pad. Furthermore, Plepys discloses a low-cost integrated circuit package with **(2)** wherein step (b) comprises: coupling a conductor to a bond pad (36) formed on the integrated circuit (32); connecting the conductor directly to the conductive layer (56). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the above teachings to manufacture a semiconductor interconnection to improve its performance.

Claims 3-5 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Broadbent (U.S. 5,063,175) in view of Manteghi (U.S. 6,228,683 B1) and further in view of Ma (U.S. 6,022,787)

Broadbent and Manteghi teach everything above except for ground and power, and signal line. However, Ma disclose a method of making an integrated circuit with **(3)**

further comprising providing one of a ground plane and a power plane in the exposed portion of the conductive layer; **(4)** further comprising providing at least one connection for a signal line in the exposed portion of the conductive layer; **(5)** further comprising providing at least one connection for a signal line in the exposed portion of the conductive layer; **(9)** further comprising: providing a contact area to a ground plane by exposing the portion of the conductive layer (see columns 4, 9, lines 33-43, lines 15-30, respectively). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the above teachings to manufacture a semiconductor interconnection to improve its performance.

Allowable Subject Matter

Claims 13-16 are allowed.

The following is a statement of reasons for the indication of allowable subject matter: The prior art does not disclose or suggest inter alia the limitations "forming a second conductive layer above the second dielectric layer and forming a cavity in the first region of the second dielectric layer to expose the first and second regions of the first conductive layer and coupling a first lead of the integrated circuit to the exposed first region and a second lead of the integrated circuit to the exposed second region".

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuong A Luu whose telephone number is (703)305-0129. The examiner can normally be reached on M-F (7:30-4:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (703)308-1323. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7722 for regular communications and (703)308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Chuong Anh Luu
Assistant Examiner

CAL
September 6, 2002

CARIDAD EVERHART
PRIMARY EXAMINER